CBCS SCHEME

USN ☐☐☐☐☐☐☐☐☐☐ **15EC32**

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Analog Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Draw the circuit diagram of common Emitter fixed bias configuration. Derive the expression for Z_i Z_o, A_v using r_e model. **(08 Marks)**

b. For the network shown in Fig. Q1 (b), determine Z_i Z_o, A_v and A_i. Given h_{ic} = 1.175 KΩ, h_{fe} = 120, h_{oe} = 20 μA/v using approximate hybrid equivalent model. **(08 Marks)**

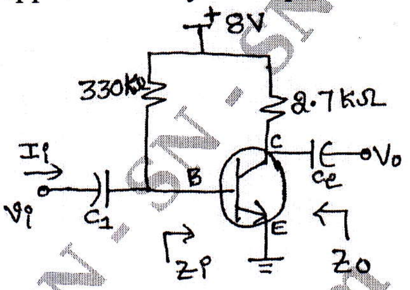

Fig. Q1 (b)

OR

2 a. Draw 'r_e' and 'h'-parameter models for a transistor in common Emitter configuration. Also give relation between 'r_e' and 'h'-parameter. **(05 Marks)**

b. For the circuit shown below, calculate r_e, Z_i Z_o and A_v, while consider $r_0 = \infty$. **(08 Marks)**

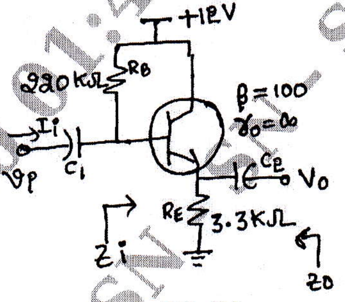

Fig. Q2 (b)

c. What are the advantages of h-parameters? **(03 Marks)**

Module-2

3 a. Explain the small signal model of the FET. **(04 Marks)**

b. Derive the expression for Z_i Z_o and A_v for FET voltage divider bias circuit. **(08 Marks)**

c. Compare JFET and MOSFET. **(04 Marks)**

OR

4 a. Explain the n-channel enhancement type MOSFETs, with their characteristics curves. **(08 Marks)**

b. Derive the expression for Z_i Z_o and A_v for FET self biased configuration (with R_s bypassed). **(08 Marks)**

Module-3

5 a. Prove that
Input capacitance is $C_{Mi} = (1 - A_v)C_f$ and
Output capacitance is $C_{MO} = \left(1 - \frac{1}{A_v}\right)C_f$ using miller effect. **(08 Marks)**

b. Describe the factors that affect the low frequency response of a BJT-CE amplifier. **(08 Marks)**

OR

6 a. Explain high frequency response of FET amplifier and derive expression for cut off frequencies, defined by input and output circuits (f_{Hi} and f_{Ho}). **(08 Marks)**

b. Determine the lower cut off frequency for the network shown in Fig. Q6 (b), using following parameters $g_m = 2$ ms, $r_d = \infty\Omega$, $I_{DSS} = 8$ mA, $V_P = -4V$, $V_{DD} = 20$ V. **(08 Marks)**

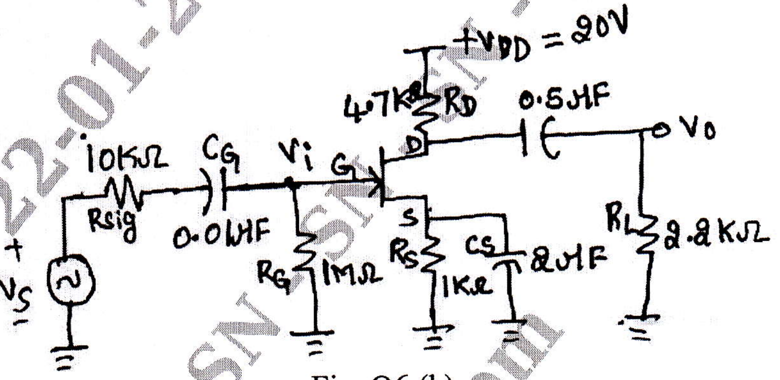

Fig. Q6 (b)

Module-4

7 a. With the help of a neat circuit diagram, explain the working of Hartley oscillator. **(08 Marks)**

b. The following data for Colpitts oscillator are as follows : $C_1 = 1$ nF, $C_2 = 99$ nF, L = 1.5 mH and $h_{fe} = 110$. Calculate frequency of oscillation for the same. **(04 Marks)**

c. Explain the important advantages of a negative feedback amplifier. **(04 Marks)**

OR

8 a. Mention the types of feedback connections. Draw their block diagrams indicating input and output signal. **(08 Marks)**

b. Obtain expression for Z_{if}, Z_{of} for a voltage series feedback. **(08 Marks)**

Module-5

9 a. Explain the operation of a class B push-pull amplifier and also show that its efficiency 78.50%. **(08 Marks)**

b. With a neat circuit diagram, explain the operation of a transformer coupled class A power amplifier. **(08 Marks)**

OR

10 a. For a harmonic distortion reading of $D_2 = 0.1$, $D_3 = 0.02$ and $D_4 = 0.01$, with $I_1 = 4$ A and $R_C = 8\ \Omega$, calculate the total harmonic distortion, fundamental power and total power. **(04 Marks)**

b. What are the classification of power amplifiers, based on the location of Q – point? Discuss them briefly. **(08 Marks)**

c. With the help of neat block diagram, explain the working of shunt voltage regulator. **(04 Marks)**

* * * * *